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On page 6, paragraph 12 has been replaced with the paragraph shown below:

Fig. 7 is a cross-sectional representation of a portion of a semiconductor substrate of another exemplary embodiment of the present invention resulting from the substrate depicted in Fig. 5 and an alternate subsequent process stage.

On pages 8 and 9, paragraph 20 has been replaced with the paragraph shown below:

Fig. 1 is a cross-sectional representation of a portion of a semiconductor substrate 10 having patterned masking material portions 17 disposed over a semiconductive material 12. Material 12 includes an outermost surface 42. Patterned masking material portions 17 encompass masking portions 16 and can also include optional pad oxide portions 14. Masking portions 16 include outermost surface 40. By way of example, patterned masking material portions 17 can be formed by forming a masking material layer (not shown) over semiconductive material 12 and then employing a photo patterning and etch process to remove portions of such masking material layer to define masking material portions 17. Where optional pad oxide portions 14 are desired, they are formed prior to the masking portions 16 and the resulting masking material portions 17 encompass both pad oxide portions 14 and masking portions 16. In some embodiments, a photoresist material employed in the photo-patterning and etch process is removed from over masking portions 16, in other embodiments, such photoresist material (not shown) is not removed. As shown, the photo patterning and etch process advantageously defines openings 20 between pairs of portions 17. Such provides but one example of forming the masking material 17 (here a composite of layers 14 and 16, with or without the photoresist material) over semiconductive material 12.

On page 12, paragraph 26 has been replaced with the paragraph shown below:

In Fig. 5, a gate dielectric comprising a first dielectric layer 60 is shown formed over semiconductive material 12 and a conductive floating gate material layer 62 is shown formed over dielectric layer 60 and STI masses 24. In the exemplary embodiment of Fig. 5, conductive floating gate material layer 62 is formed with a thickness sufficient to completely fill recess 70.

On pages 16 and 17, paragraph 35 has been replaced with the paragraph shown below:

Fig. 11 is analogous to Fig. 5 where STI masses 24 of Fig. 5 are replaced with STI masses 24c as discussed above. Thus, first dielectric layer 60c is shown formed over semiconductive material 12 and conductive floating gate material layer 62c is shown formed over dielectric layer 60 and STI masses 24c. The exemplary embodiment of Fig. 11 depicts conductive floating gate material layer 62c formed with a thickness sufficient to completely fill recess 70c.

In the Claims

Please cancel claims 1-48 without prejudice.